ABSTRACT OF THE DISCLOSURE

In a computer system that concurrently executes a plurality of tasks, a cache controller eliminates the possibility of the hit rate of one task dropping due to execution of another task. A region managing unit manages a plurality of regions in a cache memory in correspondence with a plurality of tasks. An address receiving unit receives, from a microprocessor, an address of a location in a main memory at which data to be accessed to execute one of the plurality of tasks is stored. A caching unit acquires, if the data to be accessed is not stored in the cache memory, a data block including the data from the main memory, and stores the acquired data block into a region in the cache memory corresponding to the task.